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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,018	01/03/2001	Motoshi Ito	YAMAP0748US	3434
7590 Neil A. DuChes Renner, Otto, Boisselle, & Sklar, L.L.P. 19th Floor 1621 Euclid Avenue Cleveland, OH 44115			EXAMINER HENNING, MATTHEW T	
			ART UNIT 2131	PAPER NUMBER

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/754,018

Applicant(s)

ITO ET AL.

Examiner

Matthew T. Henning

Art Unit

2131

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

This action is in response to the communication filed on 10/19/2006.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/19/2006 have been fully considered but they are not persuasive.

Regarding the applicants' argument that the cited references do not teach a portion of the single hardware circuit performing both a data scramble function and an error correction function, the examiner does not find the argument persuasive. First, the examiner notes that with regards to claim 1, the details of the circuit have not been given patentable weight, as the claim is directed towards the control program and not the circuit.

Second, the examiner further notes that as the claims are presented, a logical box around the decryption and error correction elements of Oishi still meets the newly recited claim limitation of "a portion" performing both functions. As claimed, the limitation is still a "logical" box wherein both functions are performed. Further still, the claim does not appear to be consistent with the specification in that the specification discloses a specific function (the 8-order primitive polynomial) which happens to scramble the data input for error correction, and the claim merely claims any circuit which performs both error correction and data scrambling. As such, the examiner does not find the argument persuasive.

Further note the new rejection in view of Murakami et al. presented below.

All objections and rejections not presented below have been withdrawn.

1 *Claim Rejections - 35 USC § 103*

2 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
3 obviousness rejections set forth in this Office action:

4 *A patent may not be obtained though the invention is not identically*
5 *disclosed or described as set forth in section 102 of this title, if the differences*
6 *between the subject matter sought to be patented and the prior art are such that*
7 *the subject matter as a whole would have been obvious at the time the invention*
8 *was made to a person having ordinary skill in the art to which said subject matter*
9 *pertains. Patentability shall not be negated by the manner in which the*
10 *invention was made.*
11

12 Claims 1, 3, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over
13 Hirotani (US Patent Number 5,982,887), further in view of Oishi (US Patent Number 6,907,125),
14 and further in view of Schneier (Applied Cryptography), and further in view of Elabd (US Patent
15 Number 6,526,462).

16 Regarding claim 1, Hirotani disclosed a control program for controlling an operation of a
17 microprocessor (See Hirotani Col. 4 Paragraph 3), the control program comprising a concealed
18 program (See Hirotani Col. 3 Paragraph 7), recoverable by data scramble circuit (See Hirotani
19 Col. 3 Paragraph 8) and a non-concealed program (See Hirotani Fig. 1 Element 15 wherein only
20 part of the program is encrypted). However, Hirotani failed to disclose that at least a portion of
21 the data scramble circuit is operative to perform both a data scramble function and an error
22 correction function. Hirotani also fails to disclose the use of a system on a chip design.

23 Oishi teaches that in order to protect against errors in a decryption system, error
24 correction can be combined with the decryption system by encrypting error correction codes as
25 well as the stored data and then decrypting the codes and using the codes in error correction (See
26 Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

Art Unit: 2131

1 Schneier teaches that encryption and decryption can be performed in a hardware circuit
2 (See Schneier Pages 223-225).

3 Elabd teaches that instead of using a traditional, separate component integrated circuit
4 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

5 It would have been obvious to the ordinary person skilled in the art at the time of
6 invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by
7 utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and
8 further by providing a hardware decryption circuit to be used in place of the CPU decryption.
9 This would have been obvious because the ordinary person skilled in the art would have been
10 motivated to protect the integrity of the program in a cost efficient manner, and further would
11 have been motivated to increase the speed of the decryption, increase the security of the
12 decryption, ease in the installation of the decryption method, and increase the efficiency of the
13 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
14 providing the components of the system on a single chip. This would have obvious because the
15 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
16 efficient, and less expensive product.

17 Regarding claim 3, Hirotani disclosed a device, comprising: a microprocessor (See
18 Hirotani Fig. 3 Element 21), a program memory for storing a control program for controlling an
19 operation of the microprocessor (See Hirotani Fig. 3 Element 25), the control program including
20 a concealed program (Element 25 Encrypted Section) and a non-concealed program (Element 25
21 Program section); a rewritable memory for storing a copy of the concealed program copied from
22 the concealed program stored in the program memory (See Hirotani Col. 6 Paragraph 2 and the

Art Unit: 2131

1 rejection of claim 1 above wherein it was inherent that the encrypted program was stored, at least
2 temporarily in a rewritable memory in the decryption circuit, before decryption), and a data
3 scramble circuit for recovering the concealed program stored in the rewritable memory as a
4 recovered program (See Hirotani Col. 6 Paragraphs 2-3 and the rejection of claim 1 above), but
5 failed to disclose that at least a portion of the data scramble circuit is operative to perform both a
6 data scramble function and an error correction function.

7 Oishi teaches that in order to protect against errors in a decryption system, error
8 correction can be combined with the decryption system by encrypting error correction codes as
9 well as the stored data and then decrypting the codes and using the codes in error correction (See
10 Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

11 Schneier teaches that encryption and decryption can be performed in a hardware circuit
12 (See Schneier Pages 223-225).

13 Elabd teaches that instead of using a traditional, separate component integrated circuit
14 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

15 It would have been obvious to the ordinary person skilled in the art at the time of
16 invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by
17 utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and
18 further by providing a hardware decryption circuit to be used in place of the CPU decryption.
19 This would have been obvious because the ordinary person skilled in the art would have been
20 motivated to protect the integrity of the program in a cost efficient manner, and further would
21 have been motivated to increase the speed of the decryption, increase the security of the
22 decryption, ease in the installation of the decryption method, and increase the efficiency of the

1 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
2 providing the components of the system on a single chip. This would have obvious because the
3 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
4 efficient, and less expensive product.

5 Regarding claim 6, Hirotani disclosed a method for creating a control program,
6 comprising: a program descramble step of descrambling a portion of a control program by
7 reverse scramble of a data scramble circuit in a device to be controlled, thereby creating a
8 concealed program as a portion of the control program (it was inherent in the invention of
9 Hirotani that a portion of the control program was encrypted in order for the control program to
10 have taken on the form of Element 25 in Fig. 3); and a program storing step of storing the control
11 program including the concealed program in a program memory so that the control program
12 controls an operation of a microprocessor in the device to be controlled (See Hirotani Col. 5 lines
13 39-44), but failed to disclose that at least a portion of the data scramble circuit is operative to
14 perform both a data scramble function and an error correction function.

15 Oishi teaches that in order to protect against errors in a decryption system, error
16 correction can be combined with the decryption system by encrypting error correction codes as
17 well as the stored data and then decrypting the codes and using the codes in error correction (See
18 Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

19 Schneier teaches that encryption and decryption can be performed in a hardware circuit
20 (See Schneier Pages 223-225).

21 Elabd teaches that instead of using a traditional, separate component integrated circuit
22 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

Art Unit: 2131

1 It would have been obvious to the ordinary person skilled in the art at the time of
2 invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by
3 utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and
4 further by providing a hardware decryption circuit to be used in place of the CPU decryption.
5 This would have been obvious because the ordinary person skilled in the art would have been
6 motivated to protect the integrity of the program in a cost efficient manner, and further would
7 have been motivated to increase the speed of the decryption, increase the security of the
8 decryption, ease in the installation of the decryption method, and increase the efficiency of the
9 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
10 providing the components of the system on a single chip. This would have obvious because the
11 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
12 efficient, and less expensive product.

13 Regarding claim 8, Hirotani disclosed a method for operating a control program,
14 comprising: a program copying step of copying a concealed program which is a portion of the
15 control program (See Hirotani Fig. 3 Element 25) from a program memory into a rewritable
16 memory (See rejection of claim 3 above); a program recovery step of recovering the concealed
17 program copied by the program copying step as a recovered program by a data scramble circuit
18 (See rejection of claim 3 above); and a program execution step of executing a non-concealed
19 program included in the control program and the recovered program (See Hirotani Col. 6
20 Paragraph 5), but failed to disclose that at least a portion of the data scramble circuit is operative
21 to perform both a data scramble function and an error correction function.

1 Oishi teaches that in order to protect against errors in a decryption system, error
2 correction can be combined with the decryption system by encrypting error correction codes as
3 well as the stored data and then decrypting the codes and using the codes in error correction (See
4 Oishi Col. 3 Paragraph 4 and Col. 4 – Col. 6 Line 23)

5 Schneier teaches that encryption and decryption can be performed in a hardware circuit
6 (See Schneier Pages 223-225).

7 Elabd teaches that instead of using a traditional, separate component integrated circuit
8 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

9 It would have been obvious to the ordinary person skilled in the art at the time of
10 invention to employ the teachings of Oishi and Schneier in the decryption system of Hirotani by
11 utilizing the decryption/error correction system of Oishi for the decryption of Hirotani and
12 further by providing a hardware decryption circuit to be used in place of the CPU decryption.
13 This would have been obvious because the ordinary person skilled in the art would have been
14 motivated to protect the integrity of the program in a cost efficient manner, and further would
15 have been motivated to increase the speed of the decryption, increase the security of the
16 decryption, ease in the installation of the decryption method, and increase the efficiency of the
17 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
18 providing the components of the system on a single chip. This would have obvious because the
19 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
20 efficient, and less expensive product.

21 Regarding claim 7, the combination of Hirotani, Oishi, Schneier, and Elabd disclosed that
22 the program descramble step includes the steps of: creating a non-concealed program (it was

Art Unit: 2131

1 inherent that the program was created at some point in order for the program to have been
2 encrypted and downloaded); and synthesizing the concealed program and the non-concealed
3 program into the control program (See Hirotani Fig. 3 Element 25 wherein the encrypted and
4 non-encrypted programs are together as the program stored in program memory).

5 Regarding claim 9, the combination of Hirotani, Oishi, Schneier, and Elabd disclosed a
6 program erasure step of erasing the recovered program from the rewritable memory (See
7 Hirotani Col. 6 Paragraph 6).

8 Claims 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the
9 combination of Hirotani, Oishi, Schneier, and Elabd as applied to claims 1 and 3 respectively
10 above, and further in view of Oualline ("Practical C++ Programming") and Ooi et al. (U.S.
11 Patent Number 5,226,129) hereinafter referred to as Ooi.

12 The combination of Hirotani, Oishi, Schneier, and Elabd disclosed a recoverable
13 encrypted program to be run on a microprocessor (See rejection of claim 1 above) but Hirotani
14 failed to disclose the composition of the program as well as the addressing mode of the program.
15 However, Hirotani did disclose that the encrypted program could have been downloaded over a
16 network (See Hirotani Col. 3 Lines 27-29).

17 Oualline teaches that in order to conserve memory space, commonly used code can be
18 grouped into functions such that the code can be used repeatedly (See Oualline Page 133
19 Paragraph 1). Ooi teaches that in order to easily make a program portable, the program should
20 use relative addressing (See Ooi Col. 1 Lines 27-33).

21 It would have been obvious to the ordinary person skilled in the art at the time of
22 invention to employ the teachings of Oualline to create functions in the encrypted program of

Art Unit: 2131

1 Hirotani, Oishi, Schneier, and Elabd. This would have been obvious because the ordinary person
2 skilled in the art would have been motivated to make the program as compact as possible in
3 order to conserve memory and also to limit the amount of information needing to be transferred
4 over the network to the system of Hirotani. It further would have been obvious to the ordinary
5 person skilled in the art at the time of invention to employ the teachings of Ooi in the program of
6 Hirotani, Oishi, and Schneier by providing the program with relative addressing. This would
7 have been obvious because the ordinary person skilled in the art would have been motivated to
8 minimize the modification of the code required to relocate the program, and thus increase
9 portability.

10 It would have been obvious in the combination of Hirotani, Oishi, Schneier, Elabd,
11 Oualline, and Ooi that relative address lists for the functions of the program would be provided
12 in the program at prescribed, or predetermined, location, in order for the processor of Hirotani to
13 be able to locate the functions called throughout the program.

14
15 Claims 1, 3, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over
16 Hirotani (US Patent Number 5,982,887), further in view of Murakami et al. (US Patent Number
17 5,613,005) hereinafter referred to as Murakami, and further in view of Schneier (Applied
18 Cryptography), and further in view of Elabd (US Patent Number 6,526,462).

19 Regarding claim 1, Hirotani disclosed a control program for controlling an operation of a
20 microprocessor (See Hirotani Col. 4 Paragraph 3), the control program comprising a concealed
21 program (See Hirotani Col. 3 Paragraph 7), recoverable by data scramble circuit (See Hirotani
22 Col. 3 Paragraph 8) and a non-concealed program (See Hirotani Fig. 1 Element 15 wherein only

Art Unit: 2131

1 part of the program is encrypted). However, Hirotani failed to disclose that at least a portion of
2 the data scramble circuit is operative to perform both a data scramble function and an error
3 correction function. Hirotani also fails to disclose the use of a system on a chip design.

4 Murakami teaches a particular encryption and decryption circuit which uses irreducible
5 polynomials which corrects errors during decryption in order to protect against errors or missing
6 data in a decryption system, (See Murakami Col. 1 Line 57 – Col. 2 Line 7).

7 Schneier teaches that encryption and decryption can be performed in a hardware circuit
8 (See Schneier Pages 223-225).

9 Elabd teaches that instead of using a traditional, separate component integrated circuit
10 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

11 It would have been obvious to the ordinary person skilled in the art at the time of
12 invention to employ the teachings of Murakami and Schneier in the decryption system of
13 Hirotani by utilizing the decryption/error correction system of Murakami for the decryption of
14 Hirotani and further by providing a hardware decryption circuit to be used in place of the CPU
15 decryption. This would have been obvious because the ordinary person skilled in the art would
16 have been motivated to protect the integrity of the program in a cost efficient manner, and further
17 would have been motivated to increase the speed of the decryption, increase the security of the
18 decryption, ease in the installation of the decryption method, and increase the efficiency of the
19 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
20 providing the components of the system on a single chip. This would have obvious because the
21 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
22 efficient, and less expensive product.

1 Regarding claim 3, Hirotani disclosed a device, comprising: a microprocessor (See
2 Hirotani Fig. 3 Element 21), a program memory for storing a control program for controlling an
3 operation of the microprocessor (See Hirotani Fig. 3 Element 25), the control program including
4 a concealed program (Element 25 Encrypted Section) and a non-concealed program (Element 25
5 Program section); a rewritable memory for storing a copy of the concealed program copied from
6 the concealed program stored in the program memory (See Hirotani Col. 6 Paragraph 2 and the
7 rejection of claim 1 above wherein it was inherent that the encrypted program was stored, at least
8 temporarily in a rewritable memory in the decryption circuit, before decryption), and a data
9 scramble circuit for recovering the concealed program stored in the rewritable memory as a
10 recovered program (See Hirotani Col. 6 Paragraphs 2-3 and the rejection of claim 1 above), but
11 failed to disclose that at least a portion of the data scramble circuit is operative to perform both a
12 data scramble function and an error correction function.

13 Murakami teaches a particular encryption and decryption circuit which uses irreducible
14 polynomials which corrects errors during decryption in order to protect against errors or missing
15 data in a decryption system, (See Murakami Col. 1 Line 57 – Col. 2 Line 7).

16 Schneier teaches that encryption and decryption can be performed in a hardware circuit
17 (See Schneier Pages 223-225).

18 Elabd teaches that instead of using a traditional, separate component integrated circuit
19 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

20 It would have been obvious to the ordinary person skilled in the art at the time of
21 invention to employ the teachings of Murakami and Schneier in the decryption system of
22 Hirotani by utilizing the decryption/error correction system of Murakami for the decryption of

Art Unit: 2131

1 Hirotani and further by providing a hardware decryption circuit to be used in place of the CPU
2 decryption. This would have been obvious because the ordinary person skilled in the art would
3 have been motivated to protect the integrity of the program in a cost efficient manner, and further
4 would have been motivated to increase the speed of the decryption, increase the security of the
5 decryption, ease in the installation of the decryption method, and increase the efficiency of the
6 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
7 providing the components of the system on a single chip. This would have obvious because the
8 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
9 efficient, and less expensive product.

10 Regarding claim 6, Hirotani disclosed a method for creating a control program,
11 comprising: a program descramble step of descrambling a portion of a control program by
12 reverse scramble of a data scramble circuit in a device to be controlled, thereby creating a
13 concealed program as a portion of the control program (it was inherent in the invention of
14 Hirotani that a portion of the control program was encrypted in order for the control program to
15 have taken on the form of Element 25 in Fig. 3); and a program storing step of storing the control
16 program including the concealed program in a program memory so that the control program
17 controls an operation of a microprocessor in the device to be controlled (See Hirotani Col. 5 lines
18 39-44), but failed to disclose that at least a portion of the data scramble circuit is operative to
19 perform both a data scramble function and an error correction function.

20 Murakami teaches a particular encryption and decryption circuit which uses irreducible
21 polynomials which corrects errors during decryption in order to protect against errors or missing
22 data in a decryption system, (See Murakami Col. 1 Line 57 – Col. 2 Line 7).

1 Schneier teaches that encryption and decryption can be performed in a hardware circuit
2 (See Schneier Pages 223-225).

3 Elabd teaches that instead of using a traditional, separate component integrated circuit
4 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

5 It would have been obvious to the ordinary person skilled in the art at the time of
6 invention to employ the teachings of Murakami and Schneier in the decryption system of
7 Hirotani by utilizing the decryption/error correction system of Murakami for the decryption of
8 Hirotani and further by providing a hardware decryption circuit to be used in place of the CPU
9 decryption. This would have been obvious because the ordinary person skilled in the art would
10 have been motivated to protect the integrity of the program in a cost efficient manner, and further
11 would have been motivated to increase the speed of the decryption, increase the security of the
12 decryption, ease in the installation of the decryption method, and increase the efficiency of the
13 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
14 providing the components of the system on a single chip. This would have obvious because the
15 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
16 efficient, and less expensive product.

17 Regarding claim 8, Hirotani disclosed a method for operating a control program,
18 comprising: a program copying step of copying a concealed program which is a portion of the
19 control program (See Hirotani Fig. 3 Element 25) from a program memory into a rewritable
20 memory (See rejection of claim 3 above); a program recovery step of recovering the concealed
21 program copied by the program copying step as a recovered program by a data scramble circuit
22 (See rejection of claim 3 above); and a program execution step of executing a non-concealed

1 program included in the control program and the recovered program (See Hirotani Col. 6
2 Paragraph 5), but failed to disclose that at least a portion of the data scramble circuit is operative
3 to perform both a data scramble function and an error correction function.

4 Murakami teaches a particular encryption and decryption circuit which uses irreducible
5 polynomials which corrects errors during decryption in order to protect against errors or missing
6 data in a decryption system, (See Murakami Col. 1 Line 57 – Col. 2 Line 7).

7 Schneier teaches that encryption and decryption can be performed in a hardware circuit
8 (See Schneier Pages 223-225).

9 Elabd teaches that instead of using a traditional, separate component integrated circuit
10 design, a system on chip design can be used (See Elabd Col. 1 Lines 20-59).

11 It would have been obvious to the ordinary person skilled in the art at the time of
12 invention to employ the teachings of Murakami and Schneier in the decryption system of
13 Hirotani by utilizing the decryption/error correction system of Murakami for the decryption of
14 Hirotani and further by providing a hardware decryption circuit to be used in place of the CPU
15 decryption. This would have been obvious because the ordinary person skilled in the art would
16 have been motivated to protect the integrity of the program in a cost efficient manner, and further
17 would have been motivated to increase the speed of the decryption, increase the security of the
18 decryption, ease in the installation of the decryption method, and increase the efficiency of the
19 CPU. Furthermore, it would have been obvious to utilize the teachings of Elabd in the system by
20 providing the components of the system on a single chip. This would have obvious because the
21 ordinary person skilled in the art would have been motivated to produce a smaller, faster, more
22 efficient, and less expensive product.

Art Unit: 2131

1 Regarding claim 7, the combination of Hirotani, Murakami, Schneier, and Elabd
2 disclosed that the program descramble step includes the steps of: creating a non-concealed
3 program (it was inherent that the program was created at some point in order for the program to
4 have been encrypted and downloaded); and synthesizing the concealed program and the non-
5 concealed program into the control program (See Hirotani Fig. 3 Element 25 wherein the
6 encrypted and non-encrypted programs are together as the program stored in program memory).

7 Regarding claim 9, the combination of Hirotani, Murakami, Schneier, and Elabd
8 disclosed a program erasure step of erasing the recovered program from the rewritable memory
9 (See Hirotani Col. 6 Paragraph 6).

10 Claims 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the
11 combination of Hirotani, Murakami, Schneier, and Elabd disclosed as applied to claims 1 and 3
12 respectively above, and further in view of Oualline ("Practical C++ Programming") and Ooi et
13 al. (U.S. Patent Number 5,226,129) hereinafter referred to as Ooi.

14 The combination of Hirotani, Murakami, Schneier, and Elabd disclosed a recoverable
15 encrypted program to be run on a microprocessor (See rejection of claim 1 above) but Hirotani
16 failed to disclose the composition of the program as well as the addressing mode of the program.
17 However, Hirotani did disclose that the encrypted program could have been downloaded over a
18 network (See Hirotani Col. 3 Lines 27-29).

19 Oualline teaches that in order to conserve memory space, commonly used code can be
20 grouped into functions such that the code can be used repeatedly (See Oualline Page 133
21 Paragraph 1). Ooi teaches that in order to easily make a program portable, the program should
22 use relative addressing (See Ooi Col. 1 Lines 27-33).

It would have been obvious in the combination of Hirotani, Murakami, Schneier, Elabd, Oualline, and Ooi that relative address lists for the functions of the program would be provided in the program at prescribed, or predetermined, location, in order for the processor of Hirotani to be able to locate the functions called throughout the program.

Conclusion

Claims 1-3, and 5-9 have been rejected.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2131


1 A shortened statutory period for reply to this final action is set to expire THREE
2 MONTHS from the mailing date of this action. In the event a first reply is filed within TWO
3 MONTHS of the mailing date of this final action and the advisory action is not mailed until after
4 the end of the THREE-MONTH shortened statutory period, then the shortened statutory period
5 will expire on the date the advisory action is mailed, and any extension fee pursuant to 37
6 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,
7 however, will the statutory period for reply expire later than SIX MONTHS from the date of this
8 final action.

Art Unit: 2131

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew T. Henning whose telephone number is (571) 272-3790. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Art Unit 2131
12/29/2006

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1/7/07